A New Wave Fan Out Package for Heterogeneous Integration

Walter Jau - Senior Technical Director ASE

Slowing Moore's law and never-ending product demand for multi-functionality had set a new stage for "advanced packages", since 2.5D interposer's successful solution launched with GPU & HBM in 2015. Recently "Fan Out Wafer-level PoP" (beating organic BGA) has been adopted by high-end smart phone AP design, to enjoy the thinnest profile w/ excellent interconnect performance. These progresses not only encourage packaging industry, but represent an emerging trend from diversified to converged packaging platform, after 15 years of packaging evolution since wafer- bumping first went to mass market. The industry is now eager to know how far can "Fan Out Package" penetrate into the mainstream application markets?

In this ASE session, we will try to explore the Fan Out packaging possibility to address various schemes from single die, to die-2-die, package-on-package, and even SiP module with practices. And propose one step further a more "generalized" Fan Out Package platform as building blocks to construct a new wave of heterogeneous integration solutions!

Organized by: