Silicon-Less Integrated Module (SLIM™) for Mobile Applications
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SLIM™ is designed to target the most advanced multi die fan out packaging needs. SOC deconstruction or de-partitioning can take advantage of the sub-micron routing capabilities to break large die into several smaller pieces. This die splitting approach can also lead to approaching the split with different wafer nodes, such as 10nm and 28nm in a die split vs. a single 10nm die. The high routing can also enable to side-by-side integration of advanced memories with or without the use of 3D TMV interconnections. Application space ranges from the mobile products sector to the very large FCBGA product space or anywhere very high density routing is required. The wafer level SLIM™ (W- SLIM™) is a wafer level package without package substrate with or without through mold vias (TMV) to support the mobile market. SLIM™ is processed in wafer format and utilizes many of current materials used in wafer level fan out and wafer level CSP processing. In addition, several of the key SLIM™ process steps make use of TSV wafer finishing processing, equipment and materials. Several different designs have been assembled and SLIM™ wafer level products have passed reliability tests in both a 2D and 3D package construction. This testing includes board level and component level results.

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