Overcoming the Limitation of Cell Transistor Reliability in Ultimately Scaled DRAM Beyond 20-nm

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We demonstrated how a buried-gate saddle-fin cell transistor (cell TR) is formed in a fully integrated 2ynm 4Gb DRAM using silicon migration technique by hydrogen (H2) annealing. The device is prepared by applying H2 annealing after a dry etch process to form the saddle-fin structure. It clearly shows a reduction in interface trap density with notably enhanced variable-retention-time (VRT) characteristic and reliable row-hammering immunity. Anticipating that the interface trap curing will lead to practical applications to improve the reliability of the cell TR for next generation DRAM, the H2 annealing method is believed to be a highly recommendable approach due to its process simplicity for mass production.

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