Low Temperature Dielectric Material Challenges for 3D Wafer-Level Packaging Applications

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Since its inception in 1992, the ITRS Roadmap in sync with the Moore's Law has been the backbone of the semiconductor industry's technical development. While the Roadmap has served the industry well, the challenges and limitations of downscaling has officially brought the Roadmap to its end. While the industry explores many fronts to overcome device shrinkage challenges, 3D packaging systems continue to receive attention as an alternative to improve system performance including Fan Out, 3D System on Chip, and etc. The fabrication of 3D systems may involve wafer level processing of devices on wafer support systems with temporary adhesives with low temperature tolerability. The use of novel devices that are more temperature sensitive may also limit 3D wafer level processing temperatures. Such limitations in processing temperature can lead to increased levels of hydroxides and/or hydrogen in dielectric materials making them more susceptible to electrical leakage or increase in capacitance. The deterioration of its mechanical properties can also affect the structural integrity of the films, and lead to mechanical reliability issues. This presentation will take a look at several low and extremely low temperature dielectric materials and their electrical, mechanical and chemical properties to gain an understanding of what to expect in terms of low temperature dielectric material properties and how we foresee these materials to play a role in development of future 3D packaging technology.

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