Evolution of Microstructure Signatures in Thermo-Mechanical Stressed Heterogeneously Integrated Components

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The recent advanced technology on electronic devices brought the silicon die and the component continuously to a larger size for higher functionality and signal speed. With this trend, the reliability of the solder joint, bump, micro-bump and the TSV stabilities are crucial interconnections to assure the reliability of these heterogeneously integrated packages. Components such as silicon interposer-based 2.5D packages have enabled the integration of high-performance silicon and memory in close proximity, greatly increasing the bandwidth of these devices. Within such a package, the interaction among the many sub-components and materials creates a complex thermo-mechanical response in the interconnections. In addition, such components frequently require a high-layer count and high-thickness PCB, which creates a challenge for the reliability of the solder joints. As a result, the overall reliability of PCB assembly needs to be evaluated at every level of the interconnection. In this presentation, conventional and 2.5D flip chip package were subjected to temperature cycling testing and over the duration of testing, a series of microstructure evaluation were performed at the micro-bump, solder bump, and solder joint level. Each analysis included polarized optical imaging, SEM (Scanning Electron Microscope), EBSD (Electron Backscatter Diffraction) and strain contour analysis. With these techniques, microstructure signatures were identified and localized degradation mechanisms were observed by collecting high-resolution strain / stress distribution data at critical locations. The presentation will provide insight into metallurgical processes that alter the grain structure of interconnections at different dimensions and locations, and ultimately lead us to the evolution details of the potential failure mechanisms and processes in heterogeneously integrated components.