Challenges and Innovations in Interconnect Integration for Continuation of Device Scaling and Enabling Future Devices

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The scaling of silicon-based CMOS devices has been slowing down due to multiple factors such as physical limitations, extreme complexity of integration, ever-increasing capital expenditure for R&D and manufacturing costs. While the progresses in the front end of line (FEOL) which is closely connected to device architecture stalls, the scaling in the traditional Cu-based back end of line (BEOL) interconnect technology hit roadblocks also because the resistivity of the metal lines increases rapidly when the line width scales below 20 nm. Our study estimates that overall device performance can be degraded by as much as 50% when the electrical load from BEOL is added at 5 nm technology and more for the nodes beyond. Therefore, innovations in interconnect integration are becoming more important for overall circuit performance.

Interconnect integration at nano-scale inevitably faces steep challenges in the areas such as patterning with extreme ultra violet (EUV) lithography and etching of ultra low-k dielectrics, tighter process control requirements including overlays, increasing resistance of metal lines and capacitance of the insulators as well as their reliabilities. Innovative solutions are being explored to overcome these challenges based on fundamental understanding of the physics of the scaled wiring.

For future devices beyond conventional CMOS, we need to expand the concept of interconnect integration as an enabler of enhanced functionality and improved operating characteristics. Heterogenous integration of conventional logic and memory devices are actively pursued where chip-to-chip interconnect/packaging technology plays crucial roles. In addition, embedded functionality elements such as memories in logic devices are going to improve the performance and area scaling greatly. Based on these trends, IBM predicts that the performance of AI accelerators will improve 2.5x per year. Strong multi-disciplinary knowledge base and industry level collaborations are required to address the interconnect challenges created from various future device technologies.