EUV and Evolution in Lithography on the Horizon of Logic Scaling Paradigm Change
Ryoung-han Kim, imec

The increasing need of computational processing power justifies the continuation in momentum of Moore's law that is described as increased transistor density per technology node progression. In history, the semiconductor industry has been heavily relying on photolithography technology to continue the technology node transition, which has become a significant challenge recently by the late EUV arrival, added process complexity and dramatic cost-of-ownership increase on top of other technical challenges such as achieving smaller transistor gate dimension that has already started derailing from its historical scaling rate.

Design technology co-optimization (DTCO) has been adopted as a new paradigm to assist the slow scaling transistor dimension and maintain the logic technology scaling trend. However, the lithography technology is still pressured to provide even steeper scaling in other orientation. Eventually, DTCO will be bridged into system technology co-optimization (STCO) to further continue the scaling momentum. In this talk, the role and challenge of photolithography that encloses EUV and other lithographic techniques such as tool, material, computational lithography will be discussed on top of the lithography-only, DTCO and STCO paradigm changes in high-level perspective.