High Density Package Integration by WLFO based WLSiP and WLPoP

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The industry trend for dense smart system integration on package level is targeting performance improvement, miniaturization and system cost reduction. The board moves inside the package, as more functionality on less space is the key for product success in the market. The Internet of Things/ Everything (IoT/E) is on the way. What does that mean for semiconductor packaging, assembly and test? What are the requirements? Which solutions can be provided? The IoT/E market will be wide and fragmented. Many different solutions will be needed. Flexibility and the capability to customize system solutions will be crucial. Fact is, it will be all about smart system integration, e.g. integration of MEMS/ Sensors, Connectivity, Processor, Memory and Power Management. There will not be one specific packaging technology for IoT/E, and no new "IoT/E Packaging Technology". The toolbox is here already, and further features and building blocks required to meet the needs of future IoT/E modules are under development already. That is actually good news, as the cost pressure will be high, and materialization of existing manufacturing environment, of mature and yielding packaging technologies will be a key for success. The paper will present latest development status of Wafer-Level Fan-Out (WLFO) packaging technology at NANIUM, which is enabling IoT/E module solutions, namely in the segment of wearable electronics, which seems to be the most advanced area of the IoT/E. The WLFO is based on eWLB (embedded Wafer-Level Ball Grid Array) and allows highest integration density in 2D, and is further developing to very thin 3D solutions right now. Constructions with embedded actives, discrete passives, already packaged dies and other elements, qualified and getting ready for volume production will be presented including first reliability results.

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