Optimizing Etch Processing for Multi-Patterning
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Patterning using Film deposition and Etch have extended lithography by LELE and SAxP schemes, but also bring new challenges of controlling edge placement error, pitch walking, and managing CDU/LER/LWR to ~1 nm.

Pitch walking is one of the principal sources of edge placement error. Pattern variation from the SAxP patterning process leads to CD variation and depth loading in the final structure. Intermediate mask or transfer layers can reduce the transfer of variation through the patterning process, but depositing and etching the additional layers adds cost. However, optimizing the etch process can limit the contribution to pattern variability and pitch walking. This paper will discuss the key challenges, and potential solutions for patterning fidelity through plasma etch reactor design and etch process development.

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