Advanced Computation Lithography and Lithography-Aware Design for 10nm Beyond

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Advanced computation lithography proposed as a solution for faster yield learning due to minimizing the mask and design related issues and more flexible for design rules development due to larger Process Window Optimization and relax overlay. This computation lithography has wide applications in in optical proximity correction (OPC), resolution enhancement technology (RET), design rule exploration(DRE), design for manufacturing (DFM), design-technology co-optimization (DTCO), and manufacturability enhancement. This OPC includes inverse lithography technology (ILT), source mask optimization (SMO), double-triple patterning technology (DPT & TPT) and SADP(self-aligned double patterning) and SAQP (self-aligned quadruple patterning) and coloring. Computational lithography starts to play an important role accordingly for advanced generations, especially in extending the life of 193-nm immersion patterning with the latest optical and computational explorations for 10nm beyond and EUV lithography for 7nm node beyond.

In future, pre-determine for efficient lithography options are important for lithography-aware design is very important. DTCO is a key factor to enable CMOS scaling including lithography options as well as device design options. This DTCO can reduce that 10nm beyond scaling by exploring impact on design options such as standard cells, SRAM and analog contexts. This computation lithography technology can detect and fixed after hot spot detection related with yield and cost on time for both manufacturers and designers of product. This options ensure the successful delivery of both new processes and products in semiconductor manufacturing. This is important to Improve time to market for new technology and products on time.

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