Advanced Technology for Sub-10nm Patterning

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For the past half-century, semiconductor market has been expanded continuously along with drastic bit cost reduction, mostly driven by continuous scaling of semiconductor. Historically, advancement of lithographic technology was the major enabler for the regular cadence of areal shrinkage. For the past decade, various multi-patterning technologies were introduced to assist lithography for continuous scaling. Furthermore, the concept of atomic level control was brought into various processes, enabling to enhance the patterning of complex device structure. EUV is expected as next generation lithographic light source. Multi-patterning technology will continue to act as a complementary technology, along with EUV.

There are various challenges to enable patterning at future nodes, such as placement accuracy at multiple patterning, edge roughness improvement of lines and holes, alignment of multiple layers, implementation of new materials, adoption of new lithographic technologies like EUV and DSA, and overall cost solution.

In this presentation, we will provide overview of latest integrated patterning technologies and approach to the challenges at sub-10nm generation.

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