

STT-MRAM Challenges for Applications and Mass Production**S.C. Oh, S. O. Park, K. H. Hwang, H. K. Kang and ES Jung – Samsung Electronics**

These days the information expands much bigger as we move to the era of cloud, big data, and IoT. The conventional memory sub-system no longer satisfies the system requirements due to the limitation of high density, high performance and low power consumption. Thus new kind of memory sub-system solution is strongly required. During past 20 years, new type resistive memories have been developed, but they are still staying in niche market due to lacks of cost competition and the absence of killer application.

Especially, STT-MRAM among resistive memories is a unique memory which has fast operation speed, unlimited endurance in addition to non-volatility, thus is still the only candidate for replacing DRAM as a working memory.

In this presentation, opportunities and challenges of STT-MRAM, and current issues for mass production will be reviewed. To enter the major market, STT-MRAM needs to meet the requirement such as cost, speed and power, stable operation, reliability and manufacturability. In terms of the cost, it is the most important aspect to demonstrate the scalability in MTJ (Magnetic Tunnel Junction). We will show that MTJs can be scaled down below 15nm without obvious degradation [1-3]. Another fundamental key issue is a trade-off between data retention and switching current. To overcome this challenge, MTJ stack and material design will be also discussed. Finally, manufacturability issues which include particle, throughput, uniformity, 400C thermal endurance and in-fab monitoring tool will be reviewed.

References

[1] Woojin Kim et al., "Extended scalability of perpendicular STT-MRAM towards sub-20nm MTJ node", *IEEE, IEDM*, 2011, 24.1.1 - 24.1.4.

[2] Y. Kim et al., "Integration of 28nm MJT for 8~16Gb level MRAM with full investigation of thermal stability", *IEEE, VLSI Technology*, 2011, 210 - 211.

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[3] Jeong-Heon Park et al., “Enhancement of data retention and write current scaling for sub-20nm STT-MRAM by utilizing dual interfaces for perpendicular magnetic anisotropy”, *IEEE, VLSI Technology*, 2012, 57 - 58.

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