Design, Test and Reliability Challenges of HBM for AI Applications
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HBM is based on the JEDEC-listed dynamic random access memory (DRAM) technology incorporating through-silicon via (TSV) to interconnect stacked DRAM Core (Cell) die and base (Logic) die. After the first successful launching of HBM1 based AMD's Fiji Processor, which comprises a graphics processor unit (GPU) and four HBM cubes using 2.5D fine-pitch silicon interposer technology, HBM has become an industry-wide, optimized memory solution for high-performance computing (HPC), data center and network applications targeting ML (Machine Learning) and AI (Artificial Intelligence) applications.

This presentation introduces the challenges for system integrators to adopt HBM as a high-bandwidth low-power memory solutions with small form-factor. Main topics include the reliability issues in HBM 2.5D solution related with TSVs, micro bumps, fine-pitch silicon interposer and post package DRAM cell repair scheme between HBM and SOC. The thermal and power distribution network (PDN) related HBM design issues and key approaches will be also discussed. Finally, the next generation HBM3 solution will be also briefly introduced.