Various Bonding Process for FO Technology in WLP and PLP

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Today, advanced packaging technology innovation is increasingly important for driving the enhancement of package performance, lowering cost and achieving small form factor. By looking at current smart phone market, and in future AI, AR/VR, IoT and autonomous driving with supporting by 5G communication technology, the industry is looking for more compact device with minimum power consumption. However, several decades over, the industry eventually finds difficulties to follow Moore's law, to achieve continuous Silicon node scaling with well balancing in cost profile.

Advanced packaging, in this case, becomes one of possible solution to solve this in the level of packaging assembly, by moving from SoC (Silicon-on-Chip) to SiP (System-in-package) with advanced heterogeneous integration. This "mix and match" idea enables package designer to separate the original single IC chip into different segments, in which the fabrication can only focus on specific node technology requirements that every individual segment needs.

In fact, different ways of heterogeneous integration is under developing and evolving to suit the needs in the market. For example, traditional MCM package, 2.5D configuration with interposer, EMIB structure, and, last but not less, the 2.1D approach. There can also see that FO (fan-out) technology, is one of the powerful packaging method in offering higher I/O density with reduced factor, 3D stackable capability and an ideal solution for SiP platform with embedded multi active and/or passive components, that can achieve heterogeneous or homogeneous integration with interposer-less structure.

In this presentation, different FO technologies in FOWLP, FOPLP and Embedding will be showed, in terms of package configuration, associated application, process approach, technical challenge, packaging materials and equipment that required.