Wet Process Challenges for Advanced Logic Device Fabrication
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New wet cleaning and etching techniques as well as the new chemistries are critically needed for the highly scaled FinFET with new materials, as well as new device architectures such as gate-all-around (GAA) and complimentary FET (CFET) to be integrated with several performance and scaling boosters, e.g. buried power rail (BPR), metal gate cut (MGC), self-aligned gate contact (SAGC), and fully self-aligned via (FSAV).