Graphene and 2D Layered materials; Device Application Prospect
Hyeon-Jin Shin, Research Master and Project Leader, Samsung Advanced Institute of Technology

Two dimensional (2D) layered materials are crystalline materials with layered structures, including Graphene, h-BN, and Transition Metal Di-chalcogenides (TMDs). Each of their layers is consisting of one or a few atomic layers and they form van der Waals interactions with neighboring layers. Recently, they have been studied intensively due to their extraordinary properties, such as, flexibility and transparency. In addition, they have exceptional electronic, optoelectronic, chemical and mechanical properties. For example, Graphene has high electron mobility, chemical inertness, and thermal conductivity, while TMD has high photo responsivity. Based on their properties, the 2D electron systems have long been building blocks of electronic and photonic devices.
We have been investigated 2D layered materials for Si technology, but not for the active materials. We have focused 2D layered materials as interface materials due to the chemical inertness and their atomically thin nature. Especially, Graphene has been suggested as a promising material for future interconnects because of its unique electrical and chemical properties. For instance, they are good candidates for diffusion barrier.[1] Also, they are good candidates for interface materials between metal and Si to reduce the Schottky barrier heights and contact resistance in source and drain, which is one of the most critical issues for scaling down.[2]
In this talk, we will cover and discuss the possibility of Graphene and other 2D layered materials for interconnects [3] and contact resistance reducer [4, 5] in Si technology. In addition, we will also cover adaptation of these materials into present Si integration process. The direct growth is always the key technology to make all these applications realistic, and a little prospect of wafer scale graphene and 2D material growth will also be presented.

[1] L.Li et al., “Verticle and lateral copper transport through graphene layer”, *ACS Nano*, 9 (8), 8361 (2015)
[2] K.-E. Byun et al., “Graphene for true ohmic contact at metal-semiconductor junctions”, *Nano Letters*, 13 (9), 4001 (2013)
[3] C.-S. Lee et al., “Fabrication of Metal/Graphene Hybrid Interconnects by Direct Graphene Growth and Their Integration Properties” *Adv. Electron. Mater.*, 4 (6), 1700624 (2018)
[4] M.-H. Lee et al., “Two-Dimensional Materials Inserted at the Metal/Semiconductor Interface: Attractive Candidates for Semiconductor Device Contacts” *Nano Letters*, 18 (8), 4878 (2018)
[5] S.-G. Nam et al., “Barrier height control in metal/silicon contacts with atomically thin MoS_2 and WS_2 interfacial layers” *2D Mater.*, 5 (4), 041004 (2018)