Metrology and Inspection: Challenges, Opportunities and Requirements for Advanced Logic Technology

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Scaling into smaller nodes with innovations in the transistor architecture, material and adoption of 3-D technology pose significant challenge in the inspection and metrology field.

As the resolution required for the technology proceeds beyond the detection limit of optical tools, effort to get more light per pixel with increased SNR from the tool is the key and where various noise suppression techniques are being adopted to enhance defect detection. Optical inspection is being often complemented with e-beam inspection techniques along with automated TEM technology to have faster root cause analysis.

For metrology, as edge placement error (EPE) has become a key challenge in advanced technology nodes, accurate measurement in CD, LER, and overlay has been a key enabler, and traditional metrology schemes are evolving to be used in conjunction with other innovative techniques such as machine learning to process increasing amounts of data. In addition, the appearance of 3-D technology such as finfet and 3-D integration schemes requires significant level of hybridization of conventional metrology with other techniques that includes x-ray fluorescence (XRF), x-ray photoelectron spectroscopy (XPS), scatterometry and transmission electron microscopy (TEM).

The goal of this talk is to provide a broad overview of the challenges in developing advanced technology nodes and review various development activity in metrology and inspection domain as imec proceeds into 5, 3 nm node and below.