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In-line Metrology and Defectivity for 3D-SOC Hybrid Bonding and TSV Middle Formation
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The pace of innovation in device packaging technologies has never been faster and more interesting than nowadays. Traditionally, external connections to the packaged device are enabled through long wires bonded to peripherally located bond pads. With the introduction of 3D interconnects, these connections have been significantly reduced in length, thus improving the critical Power, Performance, Area and Cost (PPAC) metrics driving improved device performance. As the 3D interconnect density is increasing exponentially, pitches need to reduce to 5µm and below. Current interconnect technologies of 3D-SIC (3D-Stacked IC), do not offer such high densities. Parallel front-end of line wafer processing in combination with wafer-to-wafer (W2W) bonding and extreme wafer thinning steps in the 3D-SOC (3D System On Chip) integration technology schemes enable the increase of 3D interconnect density. With these techniques becoming more mature and hence moving towards production worthy status, the need for highly accurate and reliable in-line metrology becomes fundamental.

This session will elaborate in-line metrology and defectivity requirements for process validation and control of TSV formation, W2W bonding, TSV reveal and microbump formation for 3D-SOC integration schemes. The increase of interconnect density imposes a decrease of the interconnect pitch dimensions and tolerances. This results in challenging requirements for measurement and inspection tools and their capabilities. These challenges will be illustrated and discussed. Finally, metrology and defectivity solutions will be presented and demonstrated how they are implemented at imec to validate and control these 3D-SOC specific processes.

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